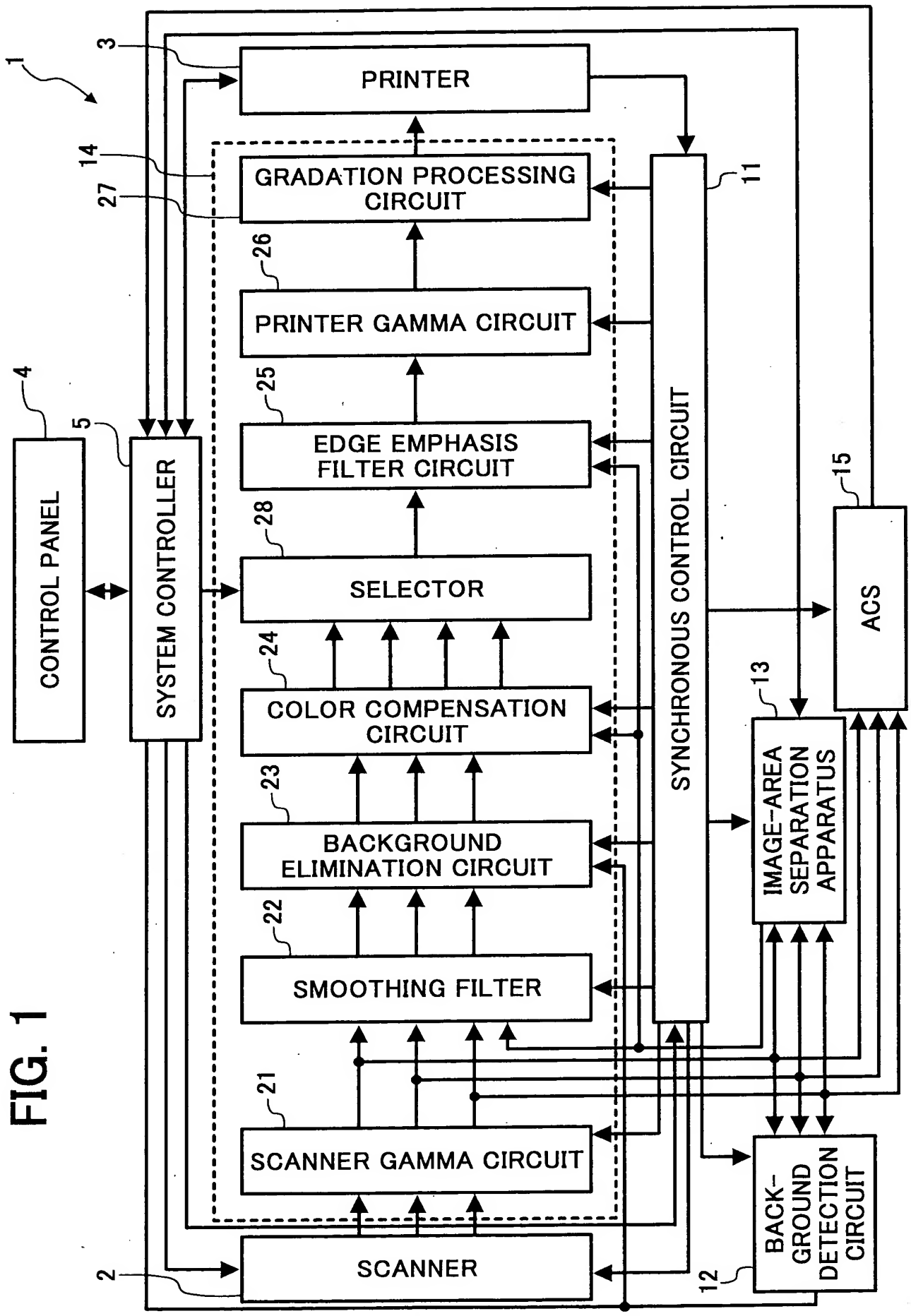
1
3
PRINTER
14
27
GRADATION PROCESSING CIRCUIT
11
26
PRINTER GAMMA CIRCUIT
4
25
EDGE EMPHASIS FILTER CIRCUIT
5
CONTROL PANEL
SYSTEM CONTROLLER
28
SELECTOR
15
ACS
24
COLOR COMPENSATION CIRCUIT
13
SYNCHRONOUS CONTROL CIRCUIT
IMAGE-AREA SEPARATION APPARATUS
23
BACKGROUND ELIMINATION CIRCUIT
22
SMOOTHING FILTER
21
SCANNER GAMMA CIRCUIT
BACK-GROUND DETECTION CIRCUIT
2
SCANNER
12

FIG. 1

FIG. 2

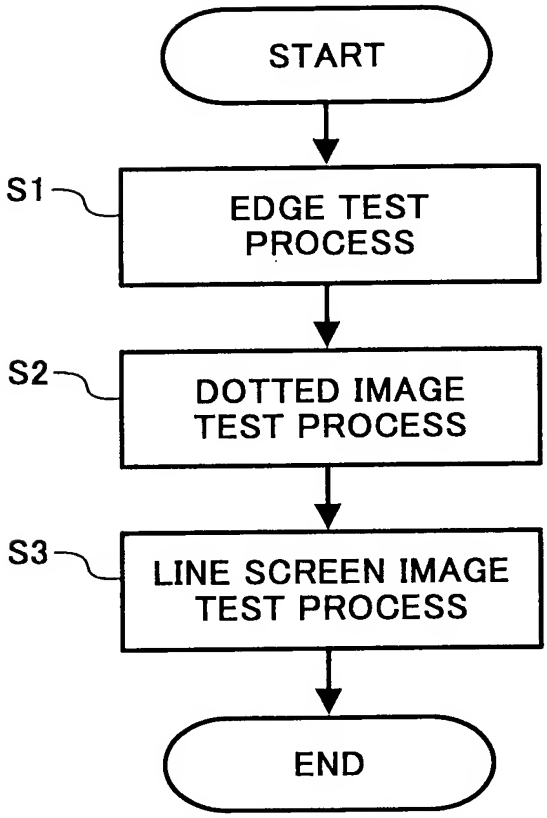
START
S1
EDGE TEST PROCESS
S2
DOTTED IMAGE TEST PROCESS
S3
LINE SCREEN IMAGE TEST PROCESS
END

FIG. 3

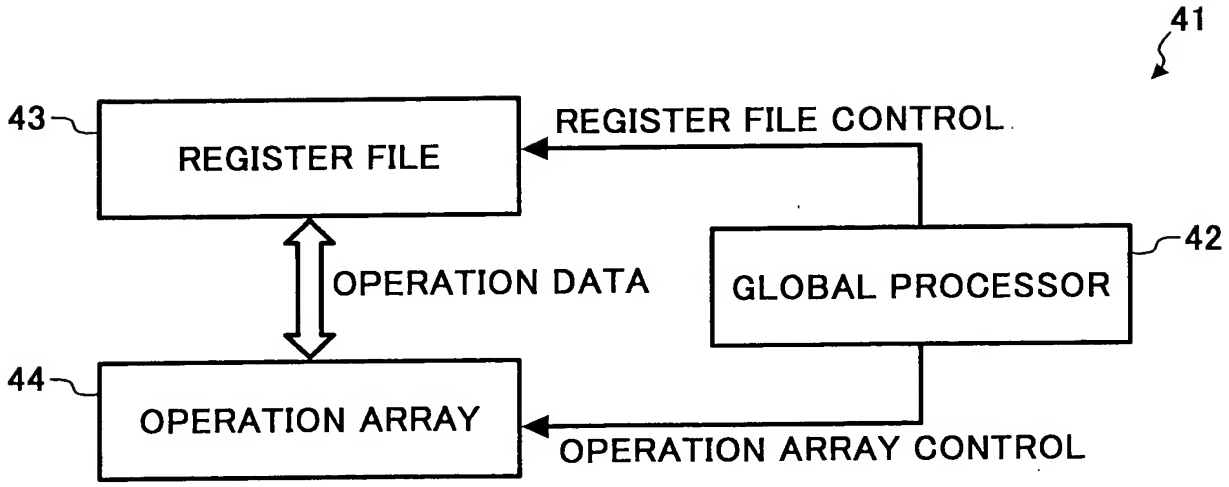
41
43
REGISTER FILE
REGISTER FILE CONTROL
OPERATION DATA
GLOBAL PROCESSOR
42
44
OPERATION ARRAY
OPERATION ARRAY CONTROL

FIG. 4

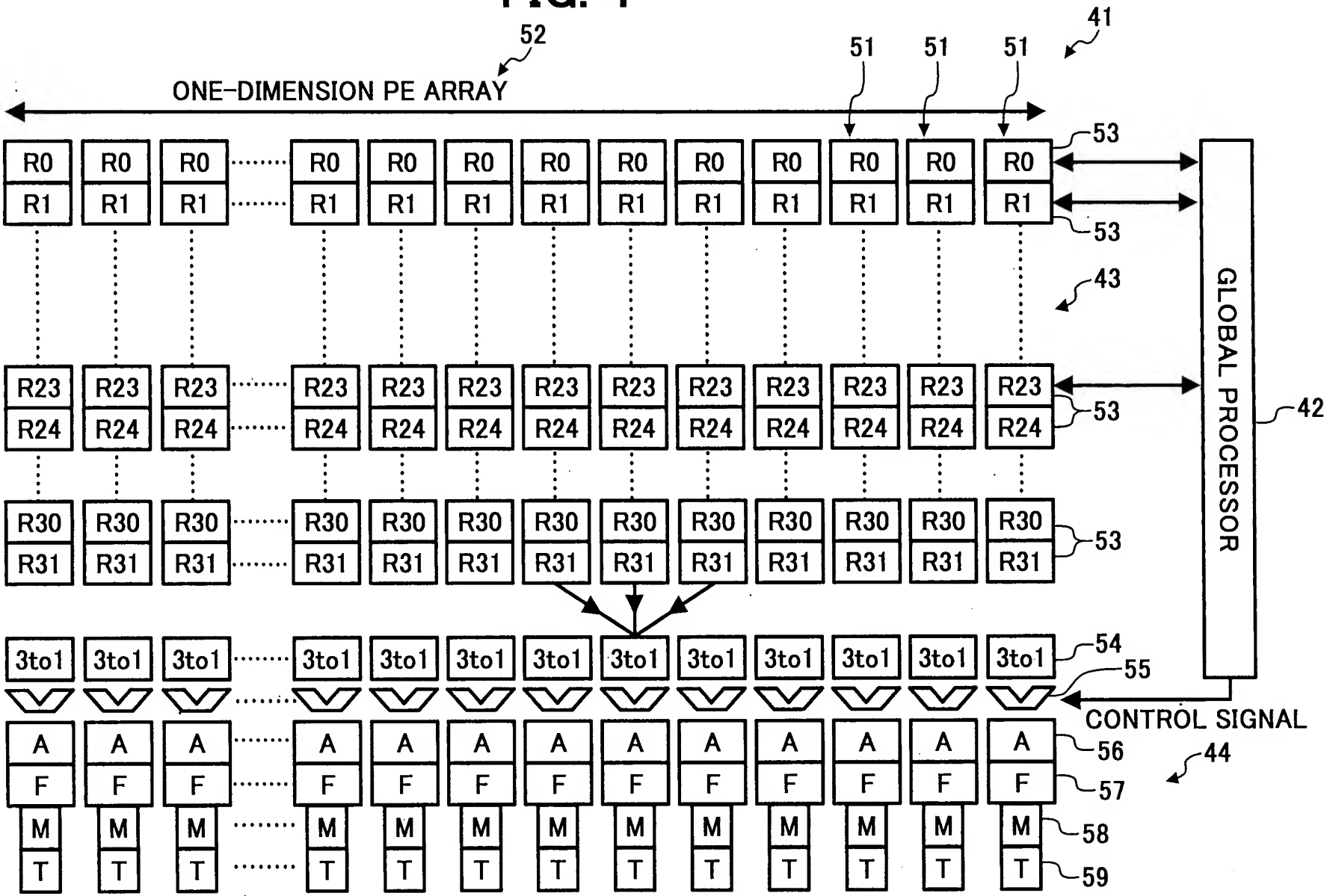
52
ONE-DIMENSION PE ARRAY
51
51
51
41
R0
R1
R23
R24
R30
R31
53
43
GLOBAL PROCESSOR
42
3to1
54
55
CONTROL SIGNAL
A
F
M
T
56
57
58
59
44

FIG. 5

f00	f01	f02
f10	f11	f12
f20	f21	f22

FIG. 6

f00	f01	f02	f03	f04
f10	f11	f12	f13	f14
f20	f21	f22	f23	f24
f30	f31	f32	f33	f34
f40	f41	f42	f43	f44

FIG. 7

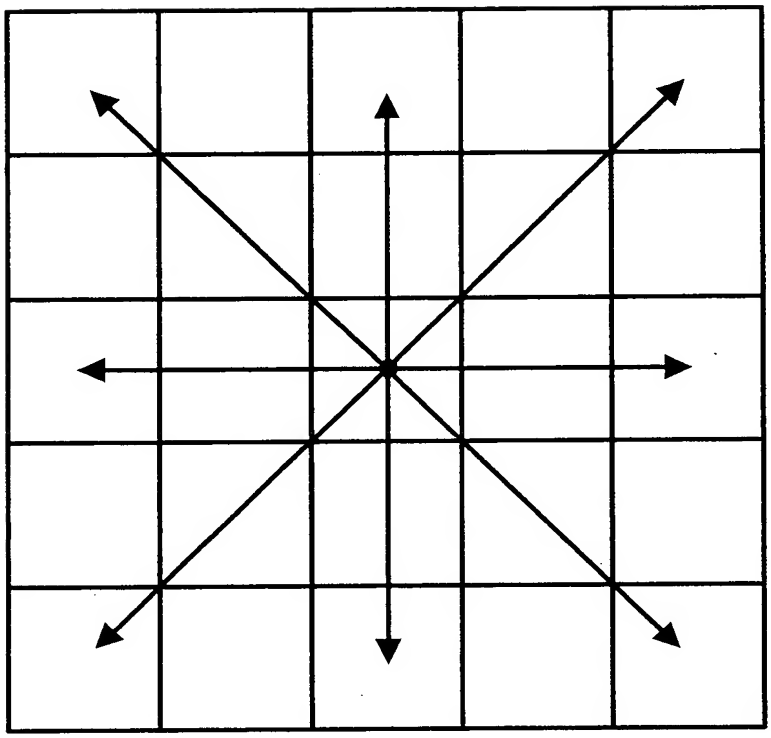

FIG. 8

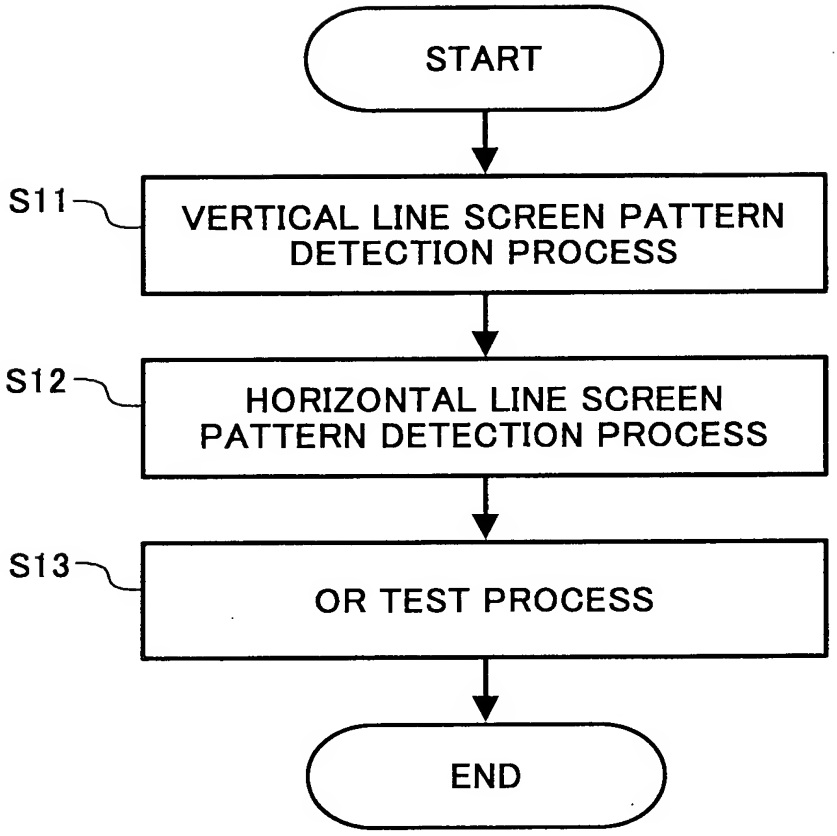
START
S11
VERTICAL LINE SCREEN PATTERN DETECTION PROCESS
S12
HORIZONTAL LINE SCREEN PATTERN DETECTION PROCESS
S13
OR TEST PROCESS
END

FIG. 9

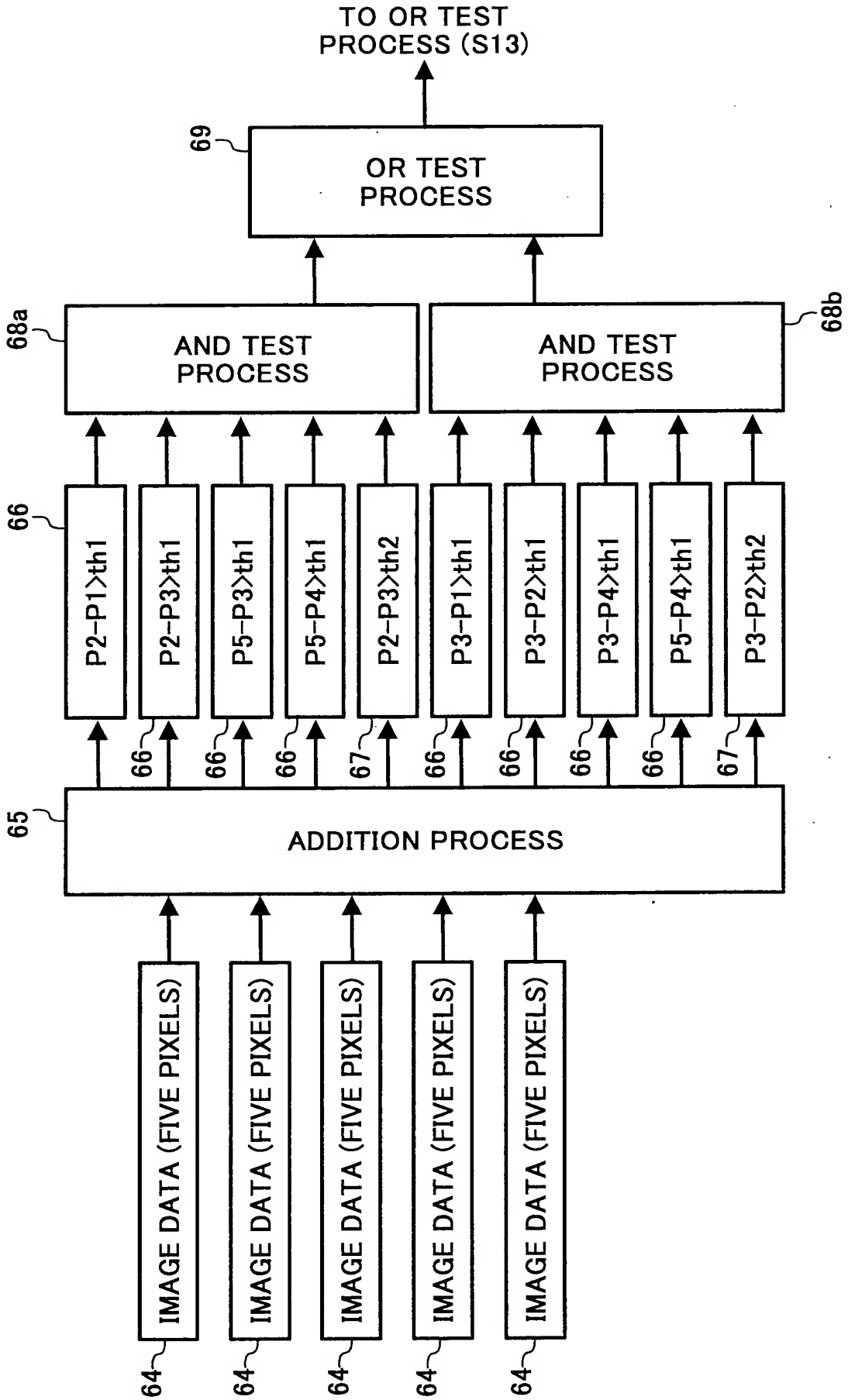
TO OR TEST PROCESS (S13)
69
OR TEST PROCESS
68a
AND TEST PROCESS
AND TEST PROCESS
68b
66
P2-P1>th1
P2-P3>th1
P5-P3>th1
P5-P4>th1
P2-P3>th2
P3-P1>th1
P3-P2>th1
P3-P4>th1
P5-P4>th1
P3-P2>th2
66
67
65
ADDITION PROCESS
IMAGE DATA (FIVE PIXELS)
64

FIG. 10A

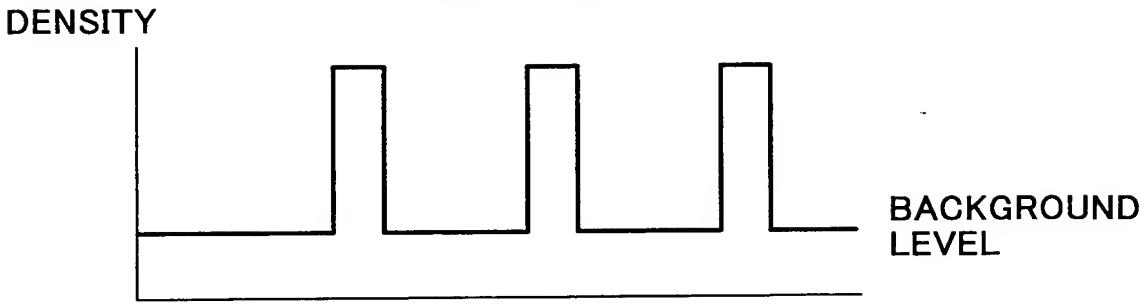

FIG. 10B

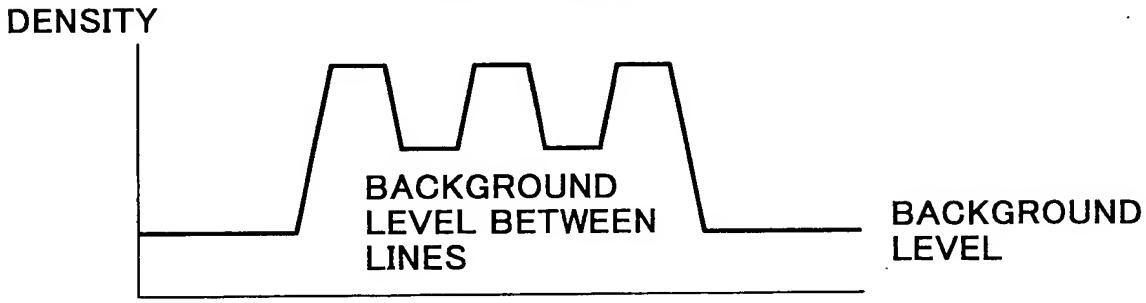

FIG. 10C

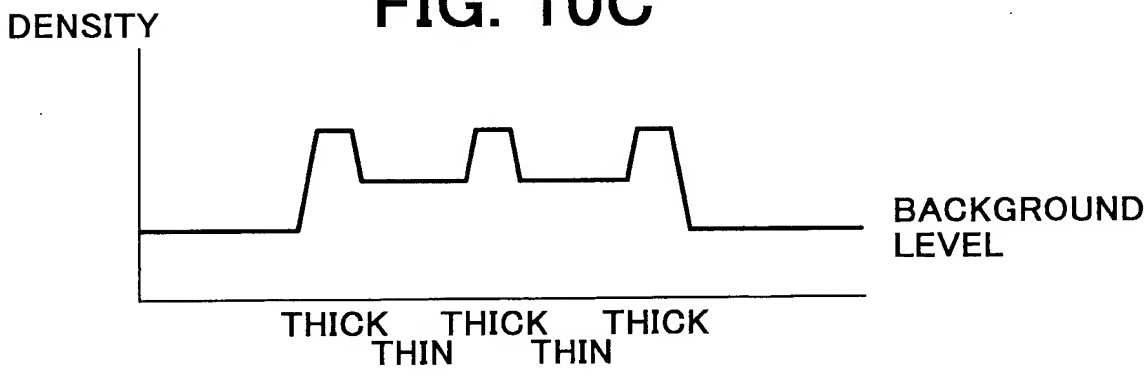

FIG. 10D

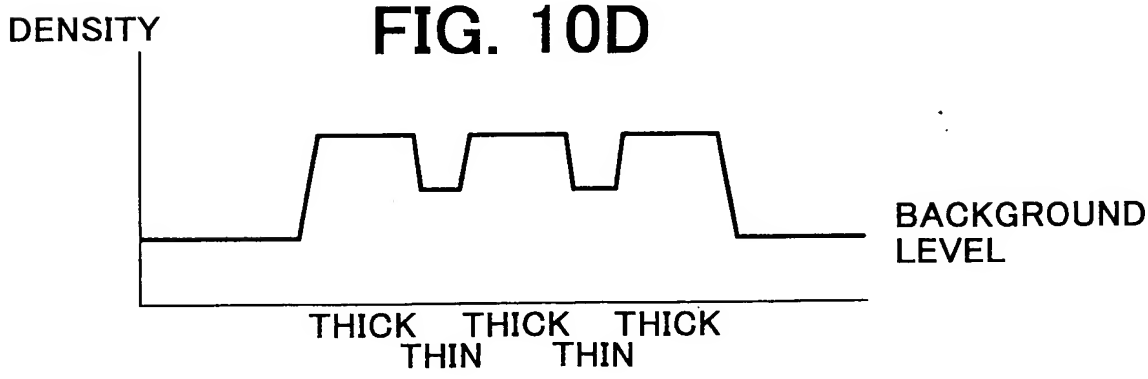

FIG. 11

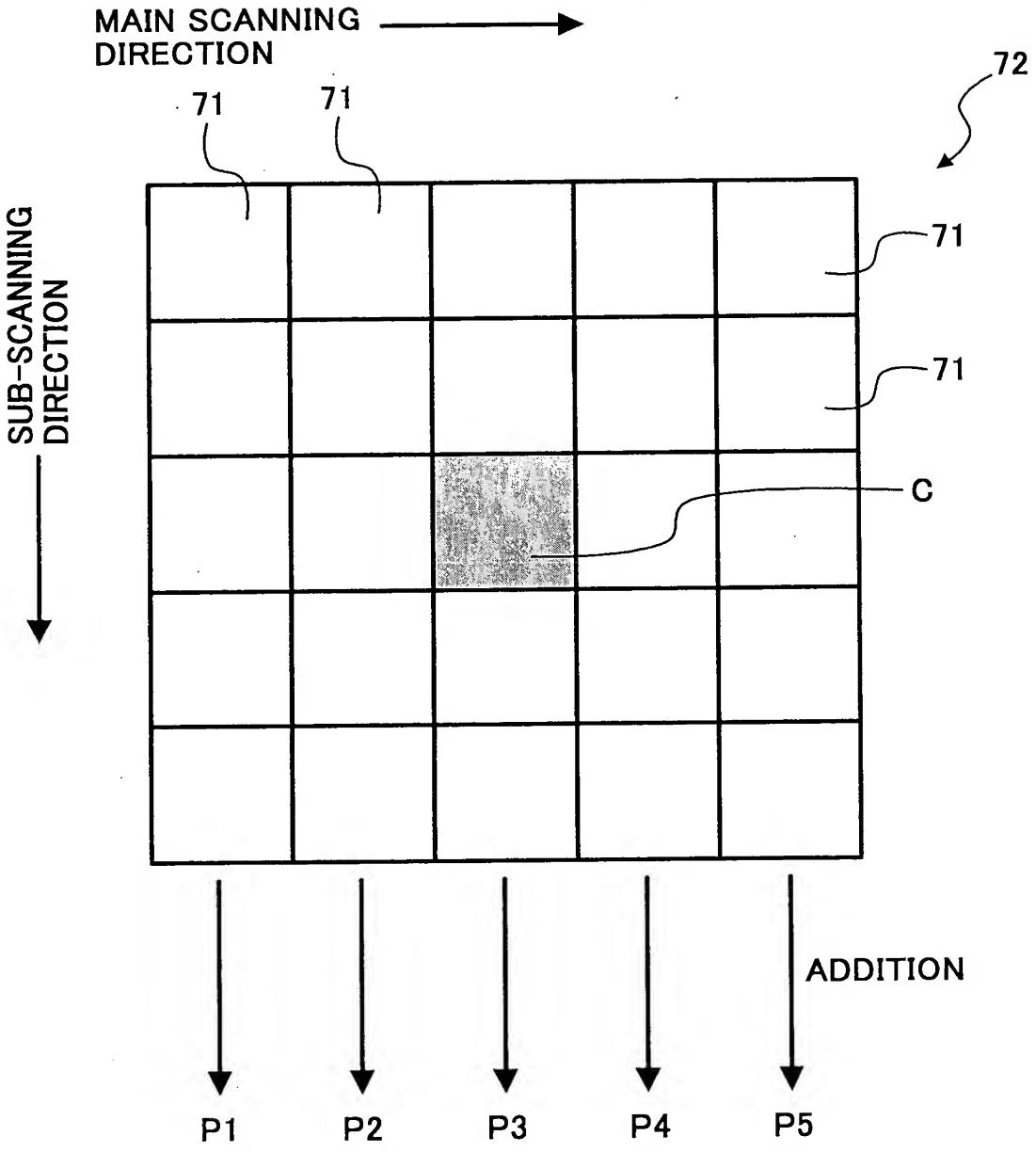
MAIN SCANNING DIRECTION
SUB-SCANNING DIRECTION
71
71
72
71
71
C
ADDITION
P1
P2
P3
P4
P5

FIG. 12

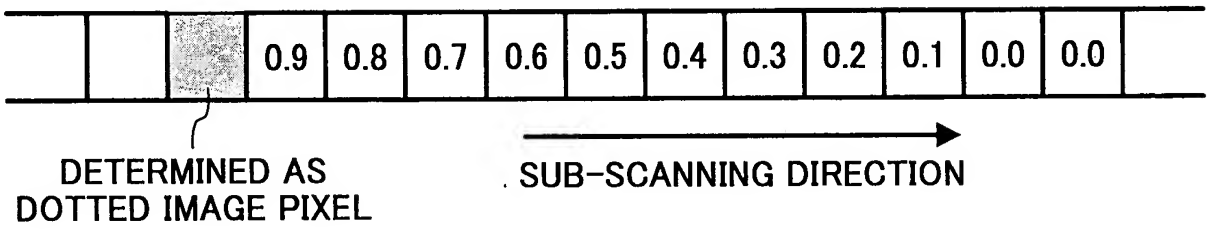
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0.0
DETERMINED AS
DOTTED IMAGE PIXEL
SUB-SCANNING DIRECTION

FIG. 13

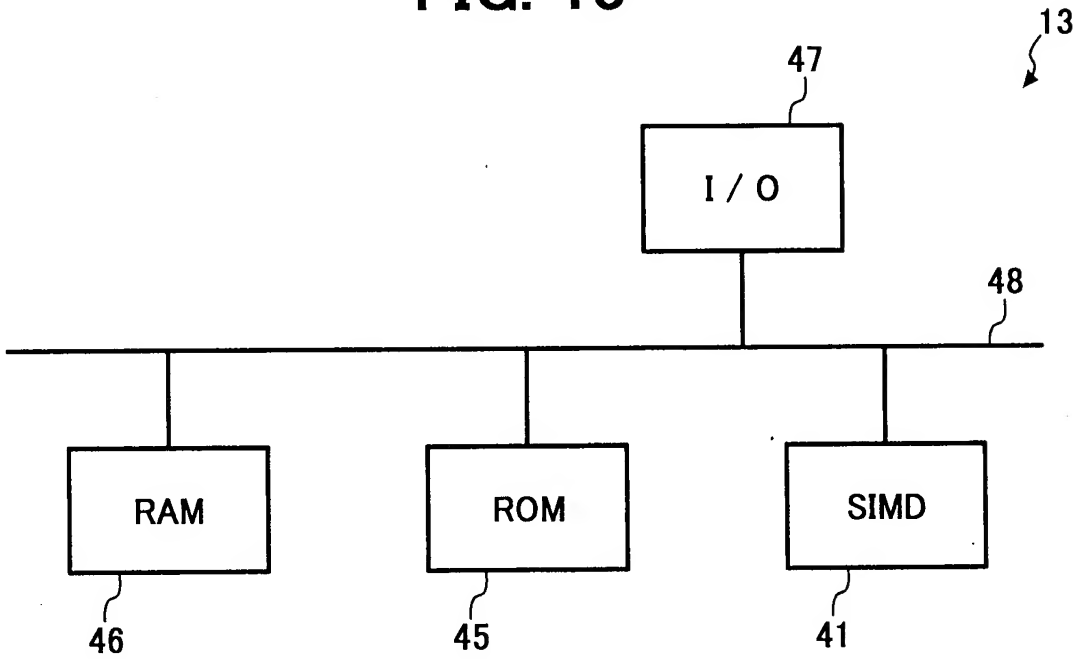
13
47
I / O
48
RAM
ROM
SIMD
46
45
41

FIG. 14A

DOTTED IMAGE PIXEL		px1	px2	px3	px4	px5	

FIG. 14B

t1		80	34	12	21	48	

FIG. 14C

DETERMINED AS DOTTED IMAGE BY t1		○	×	×	×	×	

FIG. 14D

w			0.9	0.8	0.7	0.6	

FIG. 14E

$t1_{new} = t1 * (1+w)$		80	65	23	35	78	

FIG. 14F

DETERMINED AS DOTTED IMAGE BY $t1_n$ w		○	×	×	×	○	

FIG. 15A

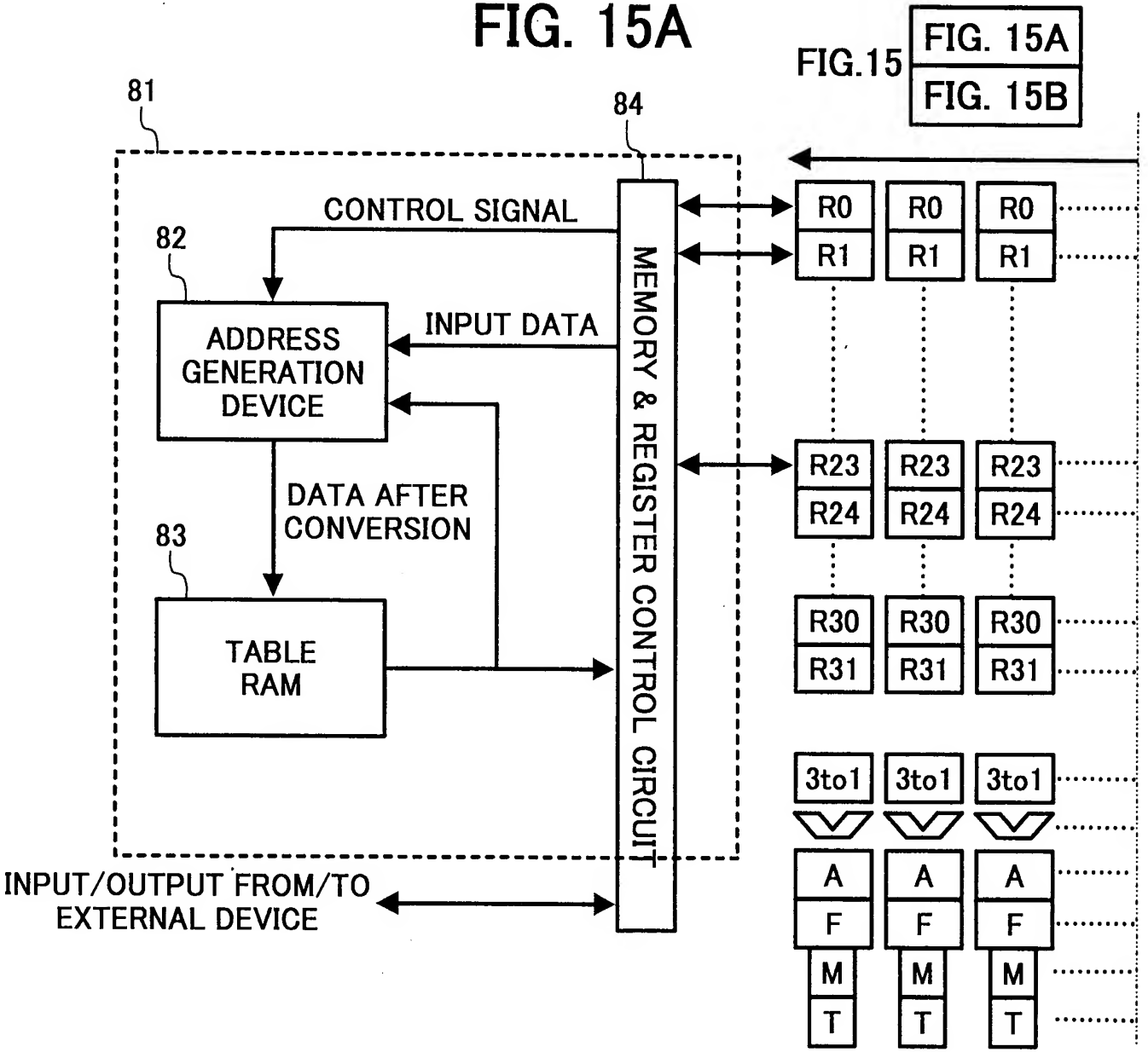
FIG.15
FIG. 15A
FIG. 15B
81
84
CONTROL SIGNAL
82
ADDRESS GENERATION DEVICE
INPUT DATA
DATA AFTER CONVERSION
83
TABLE RAM
MEMORY & REGISTER CONTROL CIRCUIT
INPUT/OUTPUT FROM/TO EXTERNAL DEVICE
R0
R1
R23
R24
R30
R31
3to1
A
F
M
T

FIG. 15B

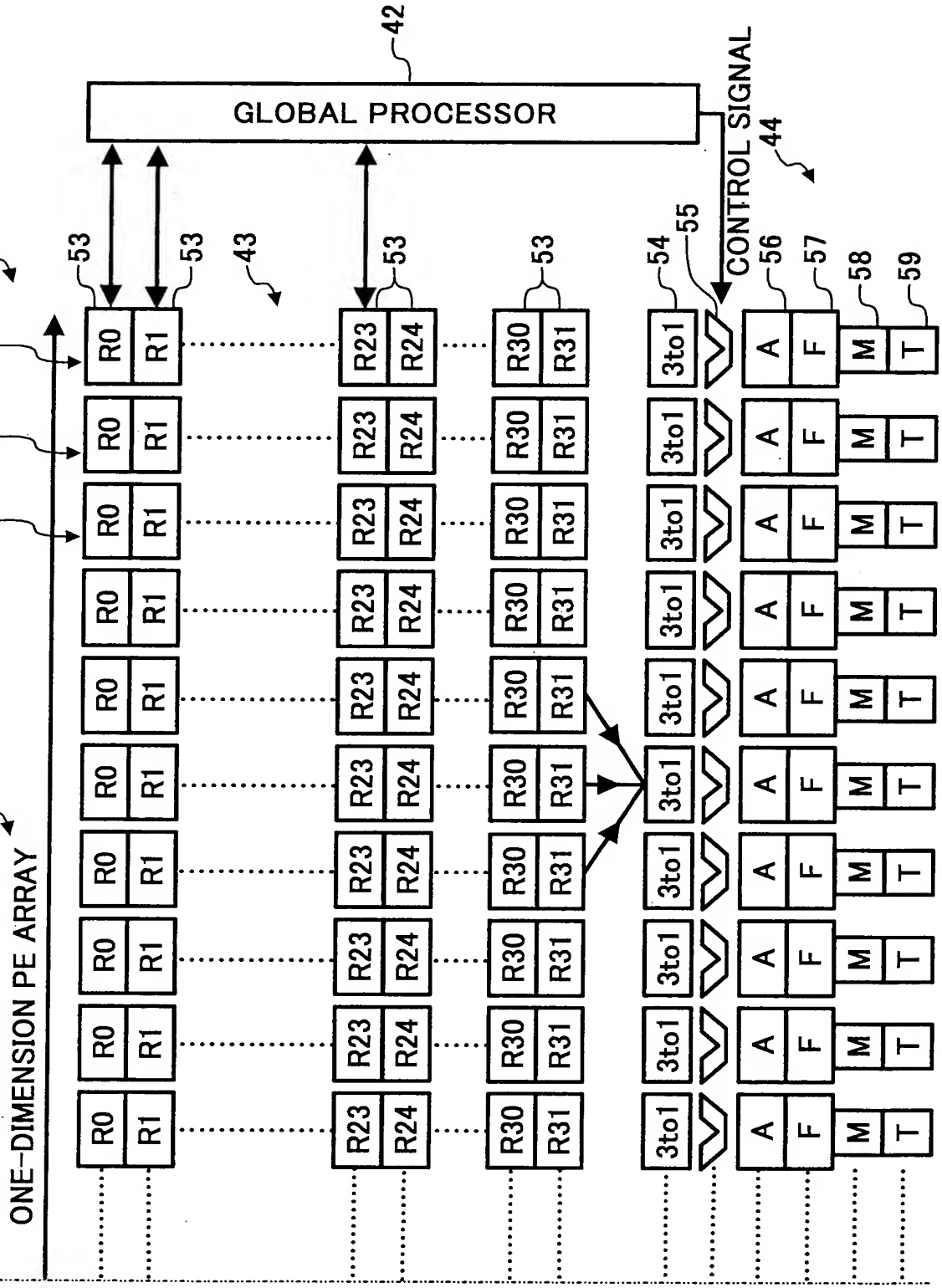
GLOBAL PROCESSOR
42
CONTROL SIGNAL
44
41
43
ONE-DIMENSION PE ARRAY
52
51
53
54
55
56
57
58
59
R0
R1
R23
R24
R30
R31
3to1
A
F
M
T

FIG. 16

STATE (4BIT)	DESCRIPTION
1010	DOTTED IMAGE TEST PIXEL BY W=0, 0t=1
1001	DISTANT BY ONE PIXEL FROM DOTTED IMAGE TEST PIXEL BY W=0.9, 0t=1
1000	DISTANT BY TWO PIXELS FROM DOTTED IMAGE TEST PIXEL BY W=0.8, 0t=1
0111	DISTANT BY THREE PIXELS FROM DOTTED IMAGE TEST PIXEL BY W=0.7, 0t=1
0110	DISTANT BY FOUR PIXELS FROM DOTTED IMAGE TEST PIXEL BY W=0.6, 0t=1
0101	DISTANT BY FIVE PIXELS FROM DOTTED IMAGE TEST PIXEL BY W=0.5, 0t=1
0100	DISTANT BY SIX PIXELS FROM DOTTED IMAGE TEST PIXEL BY W=0.4, 0t=1
0011	DISTANT BY SEVEN PIXELS FROM DOTTED IMAGE TEST PIXEL BY W=0.3, 0t=1
0010	DISTANT BY EIGHT PIXELS FROM DOTTED IMAGE TEST PIXEL BY W=0.2, 0t=1
0001	DISTANT BY NINE PIXELS FROM DOTTED IMAGE TEST PIXEL BY W=0.1, 0t=1
0000	DISTANT BY TEN OR MORE OF PIXELS FROM DOTTED IMAGE TEST PIXEL BY W=0.0, 0t=1

FIG. 17

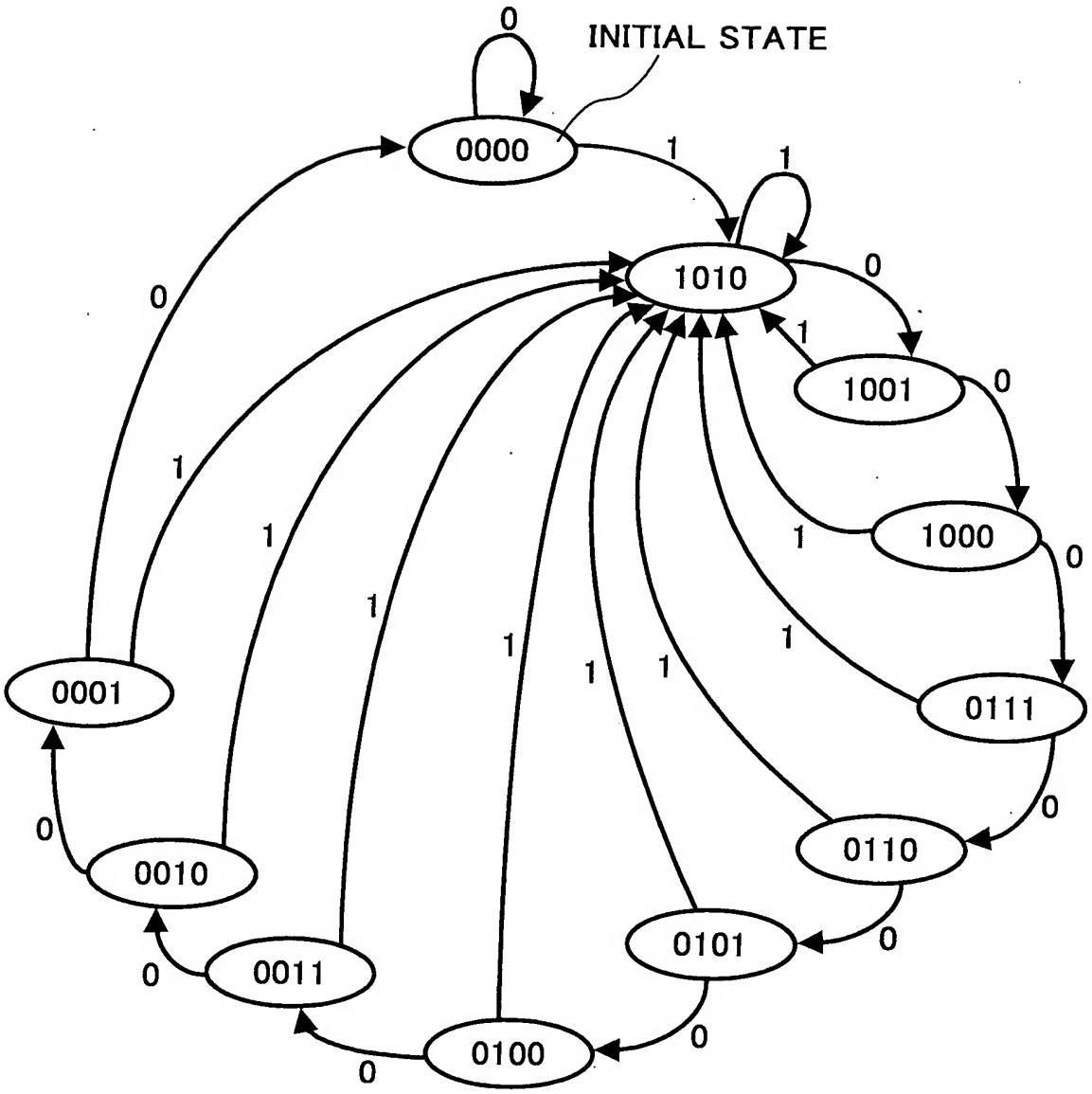
INITIAL STATE
0000
1010
1001
1000
0111
0110
0101
0100
0011
0010
0001
0
1

FIG. 18

RAM ADDRESS		EXPLANATION
PREVIOUS STATE	INPUT	NEXT STATE
0000	0	0000
0000	1	1010
0001	0	0000
0001	1	1010
0010	0	0001
0010	1	1010
0011	0	0010
0011	1	1010
0100	0	0011
0100	1	1010
0101	0	0100
0101	1	1010
0110	0	0101
0110	1	1010
0111	0	0110
0111	1	1010
1000	0	0111
1000	1	1010
1001	0	1000
1001	1	1010
1010	0	1001
1010	1	1010